Circuit Walks in Integral Polyhedra

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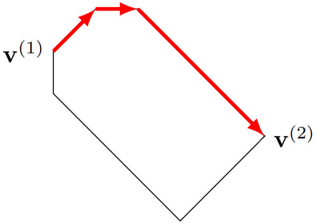
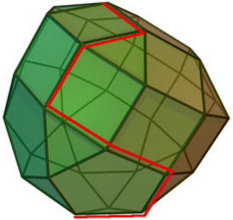
Linear Program: $\min\{\mathbf{c}^T\mathbf{x} \colon \mathbf{x} \in P\}$ where $P = \{\mathbf{x} \in \mathbb{R}^n \colon A\mathbf{x} = \mathbf{b},\ B\mathbf{x} \leq \mathbf{d}\}$.

Simplex Method: If a current vertex $\mathbf{v}$ of P is not an optimal solution, move to a neighboring vertex with improved objective value.





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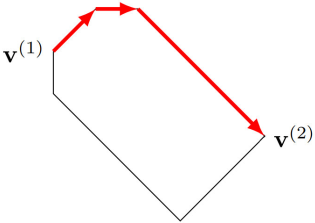

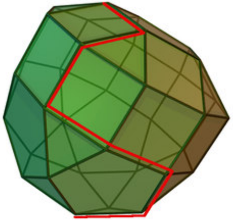

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Conjecture (Borgwardt et al., Circuit Diameter Conjecture, 2016)

*The **circuit diameter** of a d-dimensional polyhedron with f facets is at most $f - d$.*

Definition

The set of **circuits** of a polyhedron $P = \{\mathbf{x} \in \mathbb{R}^n \colon A\mathbf{x} = \mathbf{b}, B\mathbf{x} \leq \mathbf{d}\}$, denoted $\mathcal{C}(A, B)$, consists of those $\mathbf{g} \in \ker(A) \setminus \{\mathbf{0}\}$ normalized to coprime integer components for which $B\mathbf{g}$ is support-minimal over the set $\{B\mathbf{x} \colon \mathbf{x} \in \ker(A) \setminus \{\mathbf{0}\}\}$.

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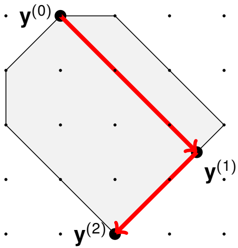
- **Circuit walks**: Generalization of edge walks in a polyhedron.
- **Circuit diameter**: Maximum number of steps needed to connect any pair of vertices in a polyhedron via a circuit walk.

Definition

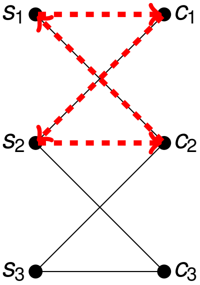
Let $P = \{\mathbf{x} \in \mathbb{R}^n \colon A\mathbf{x} = \mathbf{b}, B\mathbf{x} \leq \mathbf{d}\}$ be a polyhedron. For two vertices $\mathbf{v}^{(1)}, \mathbf{v}^{(2)}$ of P, we call a sequence $\mathbf{v}^{(1)} = \mathbf{y}^{(0)}, \ldots, \mathbf{y}^{(k)} = \mathbf{v}^{(2)}$ a **circuit walk of length** k if for $i = 0, \ldots, k-1$:

1. $\mathbf{y}^{(i)} \in P$,
2. $\mathbf{y}^{(i+1)} = \mathbf{y}^{(i)} + \alpha_i \mathbf{g}^{(i)}$ for some $\mathbf{g}^{(i)} \in \mathcal{C}(A, B)$ and $\alpha_i > 0$, and
3. $\mathbf{y}^{(i)} + \alpha \mathbf{g}^{(i)}$ is infeasible for all $\alpha > \alpha_i$.



Combinatorial interpretations of circuit walks:

- Augmenting path algorithms for max-flow problems
- Cycle canceling algorithms for min-cost flow problems
- Cyclical shifts of commodity in transportation problems
- Clustering algorithms in partition polytopes



We introduce and study a hierarchy of **integral polyhedra** based on the behavior of their circuit walks.

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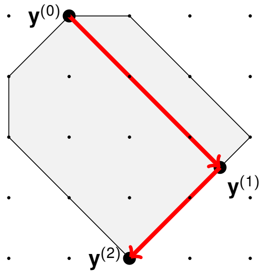
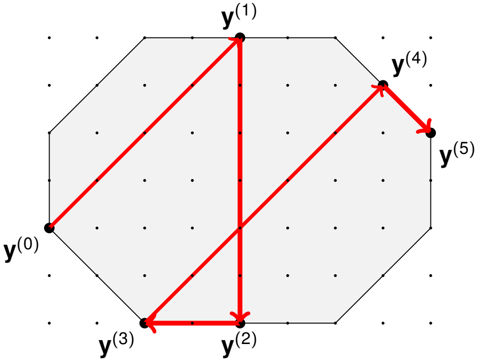
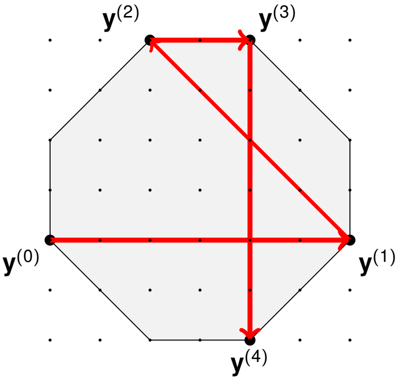
In general, circuit walks in integral polyhedra need not be integral:



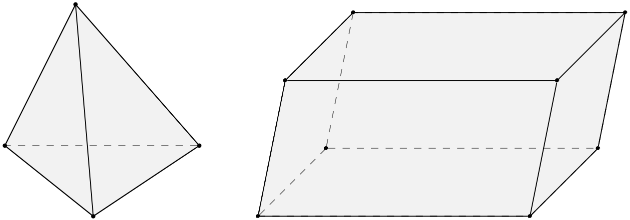
However, in certain integral polyhedra, all circuit walks are necessarily integral:

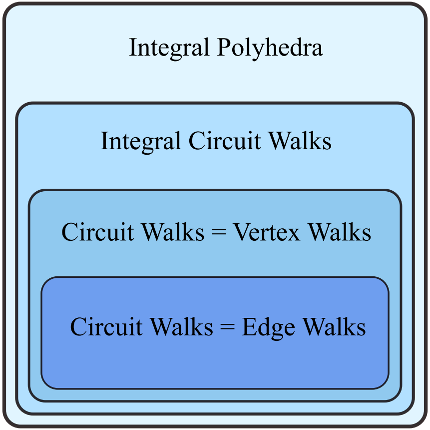


In more restrictive integral polyhedra, all circuit walks are vertex walks:



Finally, there exist integral polyhedra whose only circuit walks are edge walks:




Integral Polyhedra
Integral Circuit Walks
Circuit Walks = Vertex Walks
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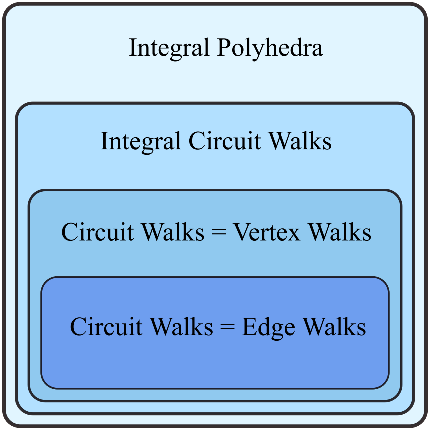

Goal: Determine where polyhedra from combinatorial optimization belong in this hierarchy.

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- 0/1-polytopes
- Polyhedra defined by totally unimodular (TU) matrices

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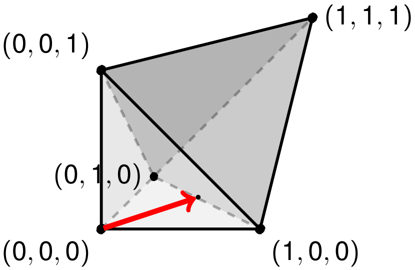

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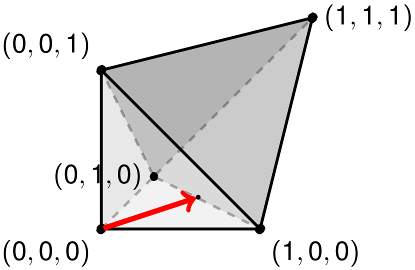

- Matroid polytopes have many non-integral circuit walks.

We say that $P = \{\mathbf{x} \in \mathbb{R}^n \colon A\mathbf{x} = \mathbf{b}, B\mathbf{x} \leq \mathbf{d}\}$ is defined by a TU matrix if the matrix $M = \binom{A}{B}$ is totally unimodular.

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- P is an integral polyhedron for any integral $\mathbf{b}, \mathbf{d}$.

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Theorem

All circuit walks in a polyhedron defined by a totally unimodular matrix are integral.

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Example: Bounded-size partition polytope $PP(\kappa^{\pm})$: a 0/1-polytope associated with the partitioning of $X = \{x_1, ..., x_n\}$ into k clusters $C_1, ..., C_k$ where $\kappa_i^- \leq |C_i| \leq \kappa_i^+$.

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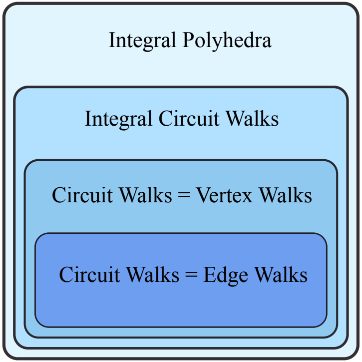
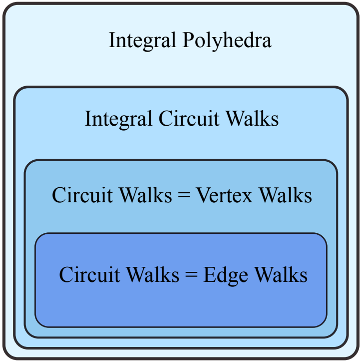
- A circuit step joins two vertices if and only if their clusterings differ by a single sequential or cyclic exchange of elements.



So far:

- Integral Polyhedron $\not\Longrightarrow$ Integral Circuit Walks
- TU Matrix $\Longrightarrow$ Integral Circuit Walks
- TU Matrix and 0/1-polytope $\Longrightarrow$ Vertex Walks



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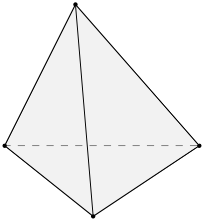
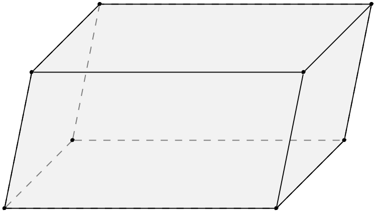
Polyhedra whose circuit walks are edge walks?





Let $P = \{\mathbf{x} \in \mathbb{R}^n \colon B\mathbf{x} \leq \mathbf{d}\}$ be a full-dimensional, non-degenerate polytope.

- Non-degenerate: each vertex $\mathbf{v}$ is contained in exactly n facets of P and is incident to exactly n edges.

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- Given two vertices $\mathbf{u}, \mathbf{v}$ of P, let P^{uv} denote the minimal face of P containing $\mathbf{u}, \mathbf{v}$, and let $I^{uv}(\mathbf{u}), I^{uv}(\mathbf{v})$ denote the inner cones of $\mathbf{u}, \mathbf{v}$ with respect to P^{uv}.

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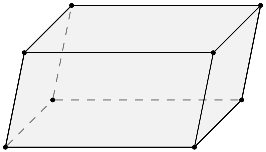
Theorem (Symmetric Inner Cone Condition)

In a non-degenerate polytope, all circuit walks are edge walks if and only if for each pair of vertices $\mathbf{u}, \mathbf{v}$, it holds that $I^{uv}(\mathbf{u}) = -I^{uv}(\mathbf{v})$.



Theorem

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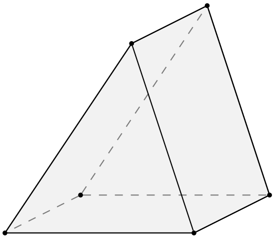

- Only non-simplex, non-parallelotope example in $\mathbb{R}^3$.

Polyhedra whose circuit walks are edge walks do appear in practice:

Example: Fixed-size partition polytope $PP(\kappa)$: associated with the partitioning of a set $X = \{x_1, ..., x_n\}$ into k clusters $C_1, ..., C_k$ in which $|C_i| = \kappa_i$ for $i = 1, ..., n$.

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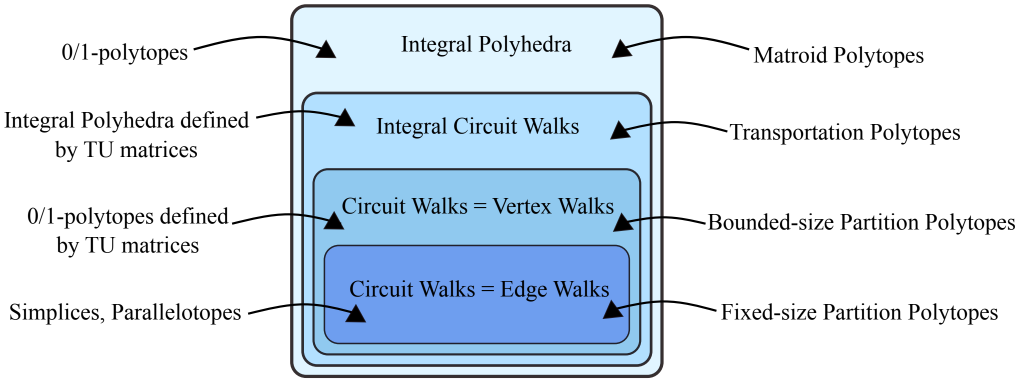
- Both edges and circuits correspond to single cyclical exchanges of elements among the clusters.
- All circuit walks are edge walks in $PP(\kappa)$.
- $PP(\kappa)$ is a highly degenerate polytope—its structure is not restricted to simplices and parallelotopes.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